REMARKS

Claims 5-10, 12-14, and 17-51 are pending. Claims 5-10, 12-14, and 17-27 have been allowed and rejected claims 1-3 and 28-30 have been deleted in favor of new claims 31-51. In addition, a Replacement Sheet has been provided to correct the omission of reference numeral 30 in Figure 1. Support for this drawing amendment may be found, for example, on page 2 of the specification.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, the Examiner rejected claims 1-3 and 28-30 under 35 USC § 102(b) for being anticipated by the Eitrheim patent. It is respectfully submitted that this rejection has been rendered moot in view of the cancellation of claims 1-3 and 28-30.

New claims 31-51 have been added to provide an additional measure of protection for the invention. Claim 31 recites a circuit having, *inter alia*, a signal processor to generate a) a first timing signal from the clock signal, b) a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay lines, and c) a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines. Support for these features may be found, for example, in Figures 1-4 of the drawings with reference to corresponding portions of the specification.

The Eitrheim patent does not teach or suggest a signal processor which generates the timing signals recited in claim 31. Dependent claims 32-41 recite additional features which are also not taught or suggested in Eitrheim.

Claim 42 recites a signal processor comprising: a first circuit to receive a first timing signal and to generate a second timing signal having edge transitions controlled by the first timing signal at times determined by a logical combination of first and second delayed clock signals, and a second circuit to generate a third timing signal having edge transitions controlled by the second timing signal at times determined by one of the first and second delayed clock signals. The Eitrheim patent does not teach or suggest a signal processor having circuits which generate these timing signals. Dependent claims 43-49 recite additional features which are also not taught or suggested in Eitrheim.

Claim 50 recites a system having features similar to those in claim 31, and claim 51 recites additional features of this system. The Eitrheim patent does not teach or suggest these features.

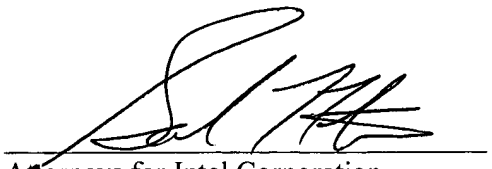
Withdrawal of all the rejections and objections of record is hereby respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and allowance of the application is respectfully solicited.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 23-1951 and please credit any

excess fees to the same Deposit Account.

Respectfully submitted,



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Amendments to the Drawings

A Replacement Sheet has been provided for Figure 1 to include a reference numeral mentioned in the specification.